SIDesigner

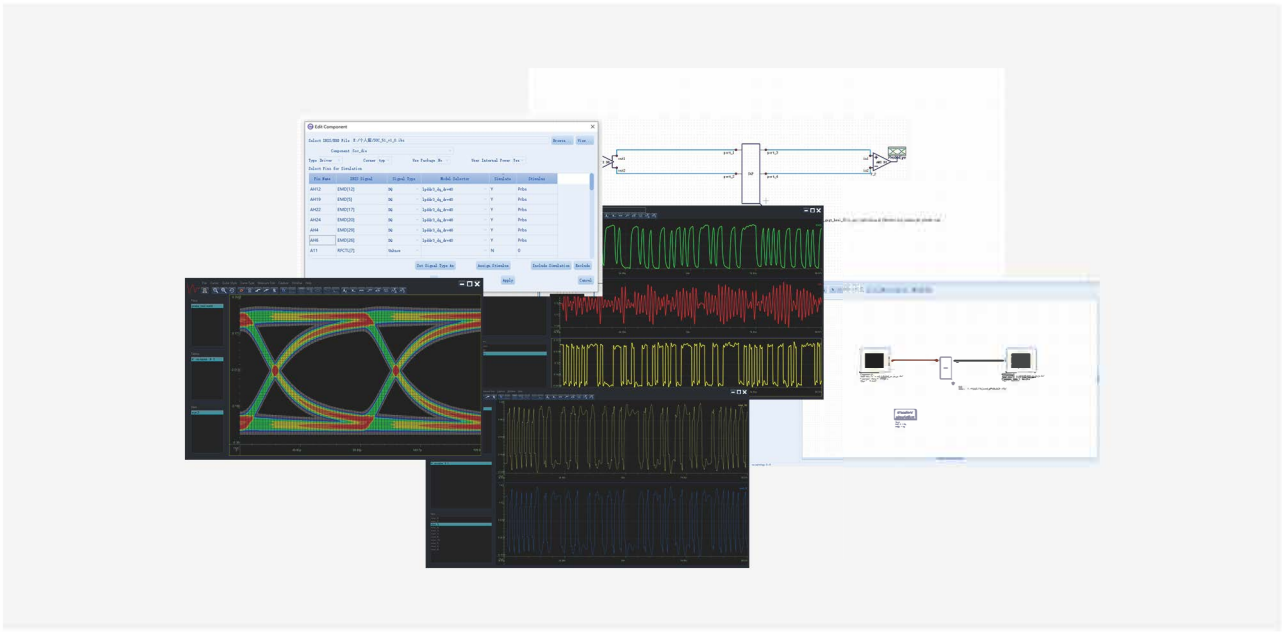
Julin-Tech Datasheet

General-Purpose Circuit Simulation Platform Focusing on Signal and Power Integrity

Overview

SIDesigner (hereinafter referred to as SIDesigner) is a GUI-based general-purpose circuit simulation platform which focuses on signal and power integrity application with built-in industry-standard SPICE engine. With SIDesigner users can set up a signal integrity or power integrity simulation by simply drag & drop operations. Besides, it also sup-ports general purpose circuit simulation, which consists of any kinds of common circuit elements.

The mission of SI Designer is to make signal integrity and power integrity analysis work easy to be done. Its ease of use flow enables the beginner to quickly get familiar with signal integrity and power integrity analysis flow, and saves the expert much flow setting time.



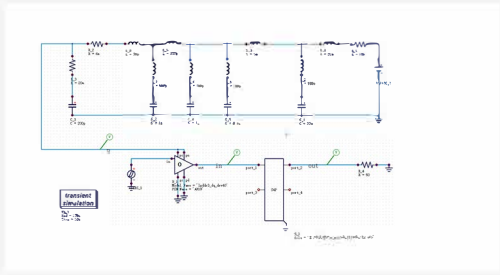
SIDesigner supports AMI, SI-PI co-simulation, DDRx verification, power-aware analysis and other main-stream fucntions. Its free-form enables the experts to perform the circuit simulation flexibly and effectively.

Key Features

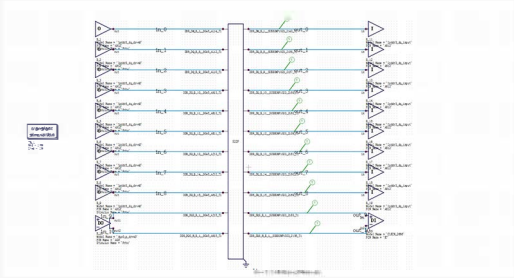
- User-friendly GUI Interface for ease of use
- Robust built-in SPICE engine without third-party SPICE license requirement
- Integrated 2D EM solver for highly accurate model of transmission lines
- Easy block building for DDR components
- Convenient setting for IBIS with easy-to-use interactive GUI
- What-if signal integrity and power integrity analysis
- General purpose circuit simulation composed of commonly used circuit elements
- Drag and drop operation to perform system-level signal integrity analysis easily
- Free-form design topologies building for quick what-if design verifications
- Built-in waveform viewer for quick simulation result check

Fuction Details

Current SIDesigner can do quick what-if analysis to get the best layout decisions in signal integrity and power integrity perspective during pre-layout stage. With the help of 3rd party 3D full-wave modeling solver, SIDesigner can do all the other signal integrity timing sign-off simulation work and SI-PI co-simulation is also supported with the help of SIDesigner's free style circuit-deck building.



SI-PI Co-SImulation



DDRx

SIDesigner supports parallel interfaces (such as DDRx, EMMC) SI analysis and Serdes channel simulation. Benefitting from free-form circuit topology building, SIDesigner can also provide power integrity analysis and other general-purpose circuit simulation.

Parallel Interfaces SI Analysis

High-speed parallel interfaces such as DDRx, EMMC, show tight design timing margin due to high cross-talk from package/PCB layout and SSN noise. SIDesigner supports all parallel interfaces' power-aware SI analysis with built-in industry-standard SPICE engine. Users can do thorough what-if digging of design parameters configuration to search for the optimal design option.

SerDes Channel Simulation

High-speed SerDes interfaces generally have BER requirements <1e-12, which needs long bit stream simulation and the efficiency is unacceptable with traditional SPICE engine. SIDesigner provides quick eye-diagrams and bathtub curves calculation to verify BER performance using industry-leading channel simulation algorithms which captures non-linear effects of the serdes system correctly.

By varying channel parameters and TX/RX IBIS AMI parameters, one can quickly evaluate channel design margin and optimal design configurations. SIDesigner supports statistical/PDA and bit by bit eye-diagram analysis for all interfaces with/without AMI model which is fairly flexible for design engineers.

Power Integrity and General-Purpose Circuit Simulation

Power noise affects timing margin greatly with interfaces' speed higher and higher. SIDesigner supports all commonly used circuit elements and power delivery network can be easily built to perform AC/DC/Transient power integrity analysis. It can also include VRM model and chip power model (CPM) for system-level power integrity analysis. By exploring different parts combinations of PDN, what-if analysis can be easily done to optimize PDN design. Besides, SIDesigner can consider power-aware effects in signal integrity analysis by including PDN parts.

With the help of free-form circuit building feature, SIDesigner supports general-purpose circuit topologies simulation. This enables the users to simulate what they want to verify and improve their design's performance while not being limited to pre-built channel blocks and topologies.

Supported Circuit Elements

- R、L、C、E、F、G、H
- S parameter/wide-band spice model
- Imported sub-circuit
- Transmission line, via
- IBIS、IBIS-AMI
- Transistor，diode
- Commonly used sources

Supported Analysis Types

- DC Analysis
- AC Analysis
- Transient Analysis
- Statistical eye-diagram analysis
- PDA (Peak Distortion Analysis)
- Bit by bit Transient Analysis

About Julin

Founded in March 2019, Julin is a provider of auxiliary software for electronic system and integrated circuit design, committed to create full-process system-level EDA products to support leading companies with simulation platform and meet the needs of cutting-edge industry in electronic system and integrated circuit design with super high-accuracy, high-speed and large-capacity solutions.

Julin Technology Co., Ltd.
Address: Building 7, 302-304 Room, Shengrong Road 88 lane, Pudong New District, Shanghai, China

Emails: sales@julin-tech.com
For more information, please visit us online at
www.julin-tech.com.cn